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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/818,906	03/28/2001	Keiichiro Wakamiya	50090-290	2402

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EXAMINER	
PAREKH, NITIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/818,906	WAKAMIYA ET AL	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (US Pat. 6159837) in view of in view of Ohtsuka et al. (US Pat. 5952718).

Regarding claim 1, Yamaji et al. disclose a semiconductor device comprising:

- a semiconductor chip/wafer (1 in Fig. 3)
- a plurality of protective insulating layers (3/5 in Fig. 3) comprising a protective coating/film (3 in Fig. 3; Col. 5, line 46) covering the surface of the chip/wafer
- a plurality of connecting conductors (4a and 6 in Fig. 3) connected to the surface of the chip/wafer and penetrating the coating layer beyond the outside surface of the coating layer, wherein the connecting conductors are connected to bumps as external terminals (8 in Fig. 3) beyond the outside surface of the coating layer,

the connecting conductors do not include wiring layers and bumps (see Fig. 3) and the connecting conductors including a plurality of connecting conductors (38/31 and 38'/31), and

- the connecting conductors including the plurality of layers formed of same material such as metal comprising a stacking of barrier metals including titanium, nickel and palladium (col. 7, line 24; Col. 5, line 52) and a solder (6/7 in Fig. 3; Col. 7, line 11; Col. 7, line 46)

(Fig. 3; Col. 7, lines 20-47; Col. 5-7).

Yamaji et al. fail to teach at least one of the connecting conductor layer being formed as a stress absorbing layer having lower hardness than the other layer.

Ohtsuka et al. teach using a plurality of conducting barrier layers/conductors (35/38/36 in Fig. 3-5c) to reduce mechanical stress in a device where one of the layers is made of stress absorbing layer such as gold (38 in Fig. 5b/5c), the gold having a lower hardness (Col. 5, line 62) than that of the other connecting conductor layer such as nickel (35 in Fig. 5b/5c- see hardness value 30-40 Hv for gold as compared to 450-500 Hv for nickel in Col. 5, lines 49-62).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one of the connecting conductor layers being formed as a stress absorbing layer having lower hardness than the other layer as taught

by Ohtsuka et al. so that the mechanical stress and chip cracking defects can be reduced and bonding can be improved in Yamaji et al's device.

3. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (US Pat. 6159837) and Ohtsuka et al. (US Pat. 5952718) as applied to claim 1 above, and further in view of Akagawa (US Pat. 5886415).

Regarding claims 2 and 3, Yamaji et al. and Ohtsuka et al. teach substantially the entire claimed structure as applied to claim 1 above, except the connecting conductor being formed from an anisotropic conductive material or a conductive material containing metal particles respectively.

Akagawa teaches a semiconductor device having connecting conductors connected to a chip surface/electrode (not numerically referenced- see connecting portion above 36/37 in Fig. 2, 3, 7 and 8) where the connecting conductors are formed of an anisotropic conductive material (38 in Fig. 2, 3, 7 and 8; Col. 4, lines 10-25) containing metal particles (39 in Fig. 2, 3, 7 and 8; Col. 1, line 40), the anisotropic conductive material being of low hardness and being functional as a shock absorbing layer to protect the chip/device (Col. 8, lines 1-5; Col. 10, lines 30-35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the connecting conductor being formed from an anisotropic conductive material or a conductive material containing metal particles as

taught by Akagawa so that the mechanical stress and chip cracking defects can be reduced and bonding can be improved in Brady et al. and Matsuda et al's device.

4. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (US Pat. 6159837) and Ohtsuka et al. (US Pat. 5952718) as applied to claim 1 above, and further in view of Khoury (US Pat. 6436802).

Regarding claims 4-6, Yamaji et al. and Ohtsuka et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Ohtsuka et al. further teach the connecting conductors being of substantially identical diameter (see 35/36/38 in Fig. 5c), but Yamaji et al. and Ohtsuka et al. fail to teach forming the connecting conductors by stacking a plurality of layers in a staggered manner, the plurality of layers of the connecting conductors being of different diameter from each other in the sequence of layers respectively.

Khoury teaches forming a staggered contactor (230 in Fig. 7A-7L) having a plurality of metal conductors/layers such as aluminum, copper, nickel, etc. on a pad/trace (232 in Fig. 7A-7L) where the plurality of metal layers are stacked in a staggered manner, the plurality of layers of the connecting conductors being of different width (W)/diameter (D) from each other in the sequence of layers respectively (see W/D of the conductors in 237, 242, 243, etc. in Fig. 7L) to expand/fan-out pitch of the contactors (Col. 8, lines 53- Col. 9, line 60; Col. 7, line 10- Col. 8, line 10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the connecting conductors by stacking a plurality of layers in a staggered manner, the plurality of layers of the connecting conductors being of substantially identical diameter or different diameter from each other in the sequence of layers respectively as taught by Khoury so that the desired spacing/pitch for the external contacts can be achieved and the bonding strength can be improved in Ohtsuka et al. and Yamaji et al's device.

5. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (US Pat. 6159837) in view of Ohtsuka et al. (US Pat. 5952718) and Chakravorty (US Pat. 6181569).

Regarding claims 7 and 8, Yamaji et al. disclose a semiconductor device comprising:

- a semiconductor chip/wafer (1 in Fig. 3)
- a plurality of protective insulating layers (3/5 in Fig. 3) comprising a protective coating/film (3 in Fig. 3; Col. 5, line 46) covering the surface of the chip/wafer
- a plurality of connecting conductors (4a and 6 in Fig. 3) connected to the surface of the chip/wafer and penetrating the coating layer beyond the outside surface of the coating layer, wherein the connecting conductors are connected to bumps as external terminals (8 in Fig. 3) beyond the outside surface of the coating layer,

the connecting conductors do not include wiring layers and bumps (see Fig. 3) and the connecting conductors including a plurality of connecting conductors (38/31 and 38'/31)

- the connecting conductors including the plurality of layers formed of same material such as metal comprising a stacking of barrier metals including titanium, nickel and palladium (col. 7, line 24; Col. 5, line 52) and a solder (6/7 in Fig. 3; Col. 7, line 11; Col. 7, line 46)

(Fig. 3; Col. 7, lines 20-47; Col. 5-7).

Yamaji et al. fail to teach:

a) the plurality of layers of the connecting conductors being formed of different material, and

b) at least one of the connecting conductor layers being formed as a stress absorbing layer having lower hardness than the other layer.

a) Chakravorty teaches a device having a plurality of the connecting conductors (321/322 and 321/323/326 in Fig. 10a-10g) connected to a pad on a chip (304 and 302 respectively in Fig. 10a-10g) where one of the plurality of layers (323 and 326 in Fig. 10d and 10g respectively) is formed from a metal/solder material or a conductive polymer material (Col. 14, lines 20-30; Col. 13, line 25- Col. 14, line 35).

b) Ohtsuka et al. teach using a plurality of conducting barrier layers/conductors (35/38/36 in Fig. 3-5c) to reduce mechanical stress in a device where one of the layers is made of stress absorbing layer such as gold (38 in Fig. 5b/5c), the gold having a lower hardness (Col. 5, line 62) than that of the other connecting conductor layer such as nickel (35 in Fig. 5b/5c- see hardness values 30-40 Hv for gold as compared to 450-500 Hv for nickel in Col. 5, lines 49-62).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the plurality of layers of the connecting conductors being formed of different material as taught by Chakravorty and at least one of the connecting conductor layers being formed as a stress absorbing layer having lower hardness than the other layer as taught by Ohtsuka et al. so that the mechanical stress and chip cracking defects can be reduced and the desired hardness and bonding strength can be achieved in Yamaji et al's device.

6. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (US Pat. 6159837), Ohtsuka et al. (US Pat. 5952718) and Chakravorty (US Pat. 6181569) as applied to claim 7 above, and further in view of Akagawa (US Pat. 5886415).

Regarding claims 9 and 10, Yamaji et al., Ohtsuka et al. and Chakravorty teach substantially the entire claimed structure as applied to claim 7 above, except the

connecting conductor being formed from an anisotropic conductive material or a conductive material containing metal particles respectively.

Akagawa teaches a semiconductor device having connecting conductors connected to a chip surface/electrode (36 in Fig. 2, 3, 7 and 8) where the connecting conductors are formed of an anisotropic conductive material (38 in Fig. 2, 3, 7 and 8; Col. 4, lines 10-25) containing metal particles (39 in Fig. 2, 3, 7 and 8; Col. 1, line 40), the anisotropic conductive material being of low hardness and being functional as a shock absorbing layer to protect the chip/device (Col. 8, lines 1-5; Col. 10, lines 30-35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the connecting conductor being formed from an anisotropic conductive material or a conductive material containing metal particles as taught by Akagawa so that the mechanical stress and chip cracking defects can be reduced and bonding can be improved in Chakravorty, Ohtsuka et al. and Yamaji et al's device.

7. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (US Pat. 6159837), Ohtsuka et al. (US Pat. 5952718) and Chakravorty (US Pat. 6181569) as applied to claim 7 above, and further in view of Khoury (US Pat. 6436802).

Regarding claims 11-13, Yamaji et al. and Ohtsuka et al. and Chakravorty teach substantially the entire claimed structure as applied to claim 7 above, wherein Ohtsuka et al. further teach the connecting conductors being of substantially identical diameter (see 35/36/38 in Fig. 5c), but Yamaji et al., Ohtsuka et al. and Chakravorty fail to teach forming the connecting conductors by stacking a plurality of layers in a staggered manner, the plurality of layers of the connecting conductors being of different diameter from each other in the sequence of layers respectively.

Khoury teaches forming a contactor (230 in Fig. 7A-7L) having a plurality of metal conductors/layers such as aluminum, copper, nickel, etc. on a pad/trace (232 in Fig. 7A-7L) where the plurality of metal layers are stacked in a staggered manner, the plurality of layers of the connecting conductors being of different width (W)/diameter (D) from each other in the sequence of layers respectively (see W/D of the conductors in 237, 242, 243, etc. in Fig. 7L) to expand/fan-out pitch of the contactors and external contacts (Col. 8, lines 53- Col. 9, line 60; Col. 7, line 10- Col. 8, line 10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the connecting conductors by stacking a plurality of layers in a staggered manner, the plurality of layers of the connecting conductors being of substantially identical diameter or different diameter from each other in the sequence of layers respectively as taught by Khoury and Ohtsuka et al. so that the desired spacing/pitch for the external contacts can be achieved and the bonding strength can be improved in Yamaji et al's device.

Response to Arguments

8. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP
02-23-04

EDDIE LEE
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